**Lab 4: Arithmetic Circuits**

**ITI 1100 C – Digital Systems 1**

**Winter 2016**

**School of Electrical Engineering and Computer Science**

**University of Ottawa**

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**Lab 4: Arithmetic Circuits**

**Objectives**

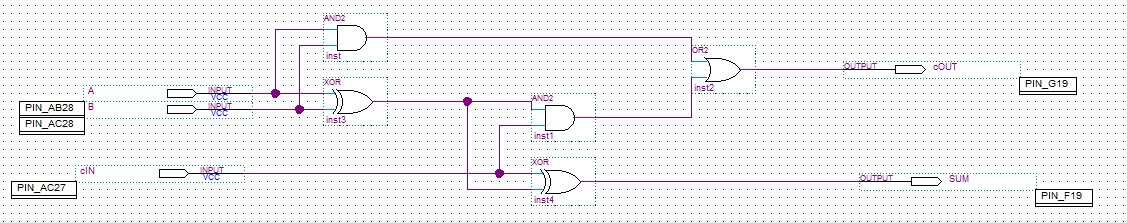
* Create and simulate a full adder, assign pins to the design, and test it on the Altera DE2-115 circuit board
* Use a full adder as a component in an 8-bit adder/subtractor
* Create a hierarchical design, including components for full adders and seven-segment decoders, using the QUARTUS II graphic editor
* Design an overflow detector for use in a two’s complement adder/subtractor

**Equipment and Components**

* Quartus II 13.0 Service-Pack 1 Software (64-bit)
* Altera DE2-115 circuit board
* Altera DE2-115 chip (EP4CE115F29C7N)

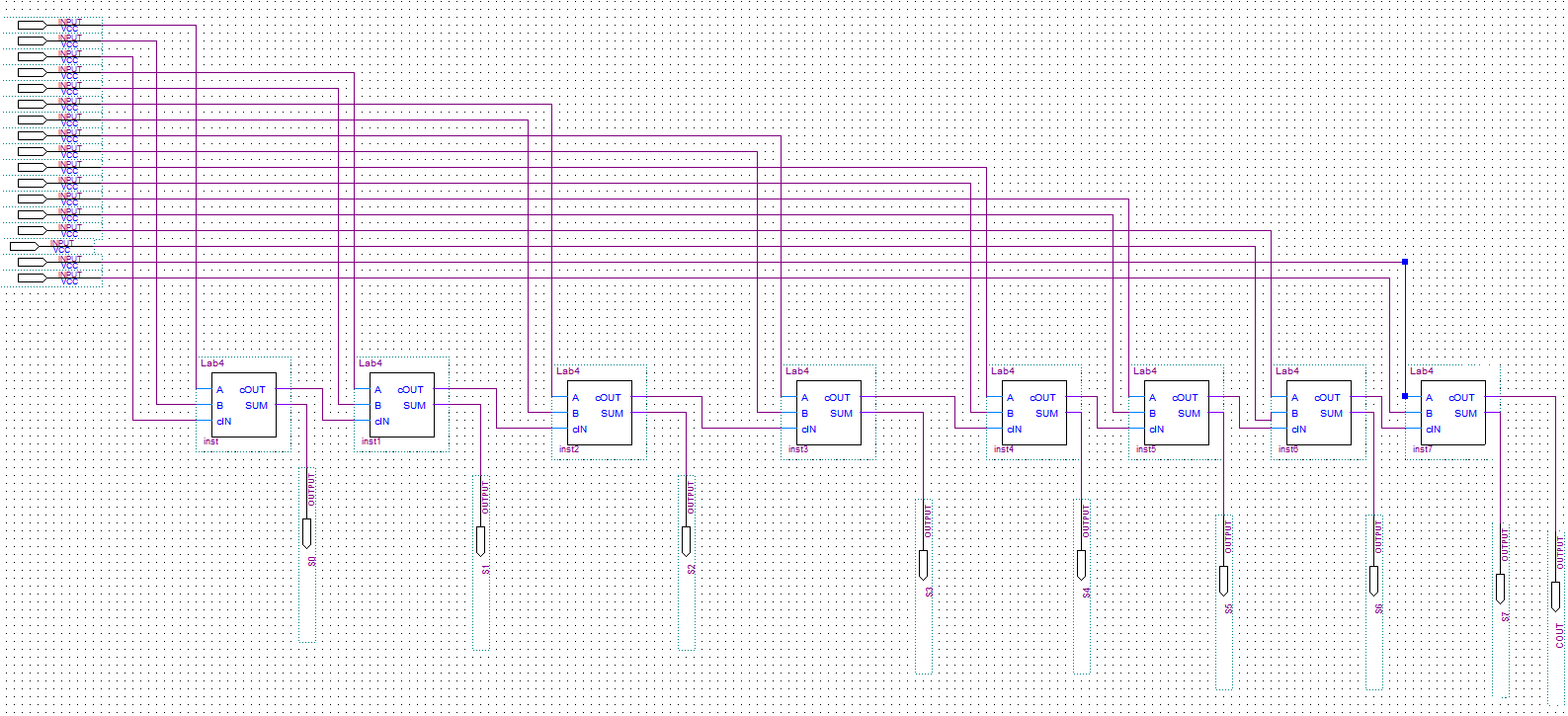
**Circuit Diagrams**

**Part 1 – Full Adders**

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**Figure 1.1:** Screen-shot of a full adder circuit diagram.

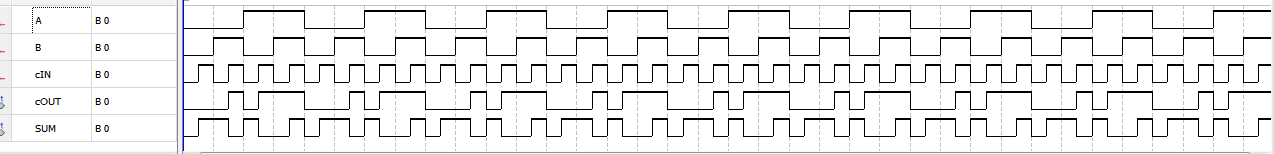
**Part II – Parallel Adder**

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**Figure 2.1:** Screen-shot of a parallel adder circuit diagram.

**Experimental Data and Data Processing**

**Part I – Full Adders**



**Figure 1.2:** Screen-shot of the simulation output of the full adder circuit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Given Input** | | | **Observed Output** | |
| **A** | **B** | **Cin** | **Cout** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Table 1.3:** Truth table for the full adder circuit.

**Part II – Parallel Adder**

(Waveform attached on next page)

|  |  |  |  |
| --- | --- | --- | --- |
| **Binary Input** | **Carry** | **Binary Sum** | **Hexadecimal Equivalent** |
| 01111111 + 00000001 | 0 | 10000000 | (7F)16 + (01)16 = (80)16 |
| 11111111 + 00000001 | 1 | 00000000 | (FF)16 + (01)16 = (00)16 |
| 11000000 + 01000000 | 1 | 00000000 | (C0)16 + (40)16 = (00)16 |
| 11000000 + 10000000 | 1 | 01000000 | (C0)16 + (80)16 = (40)16 |

**Table 1.3:** Sample sums for the 8-bit parallel adder.

**Comparison of Theoretical Data and Experimental Data**

**Part 1 – Full Adders**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Expected Results** | | **Actual Results** | |
| **A** | **B** | **Cin** | **Cout** | **Sum** | **Cout** | **Sum** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 1.4:** Comparison of the theoretical and experimental results for the full adder circuit.

The results obtained experimentally for the full adder circuit matched the results computed theoretically. This adheres to the rules of addition in base 2. (binary)

**Part II – Parallel Adder**

The results obtained experimentally for the parallel adder circuit matched the results computed theoretically. This adheres to the rules of addition in base 2. (binary)

**Part III – Two’s Complement Adder/Subtractor**

Due to time constraints, we were unable to complete the simulation for part III. The results computed theoretically are as follows.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Binary Input** | **Overflow** | **Carry** | **Binary Sum** | **Hexadecimal Equivalent** | **Two’s Compl.** |
| 01111111 + 00000001 | 1 | 0 | 10000000 | (-00)16 | 11000000 |
| 11111111 + 00000001 | 0 | 1 | 00000000 | (00)16 | 01000000 |
| 00000000 - 00000001 | 0 | 0 | 11111111 | (-7F)16 | 10000001 |
| 00000000 - 01111111 | 0 | 0 | 10000001 | (-01)16 | 11111111 |
| 11000000 + 01000000 | 0 | 1 | 00000000 | (00)16 | 01000000 |
| 11000000 + 10000000 | 1 | 1 | 01000000 | (40)16 | 01000000 |

**Table 1.5:** Sample sums and differences for an 8-bit adder/subtractor.

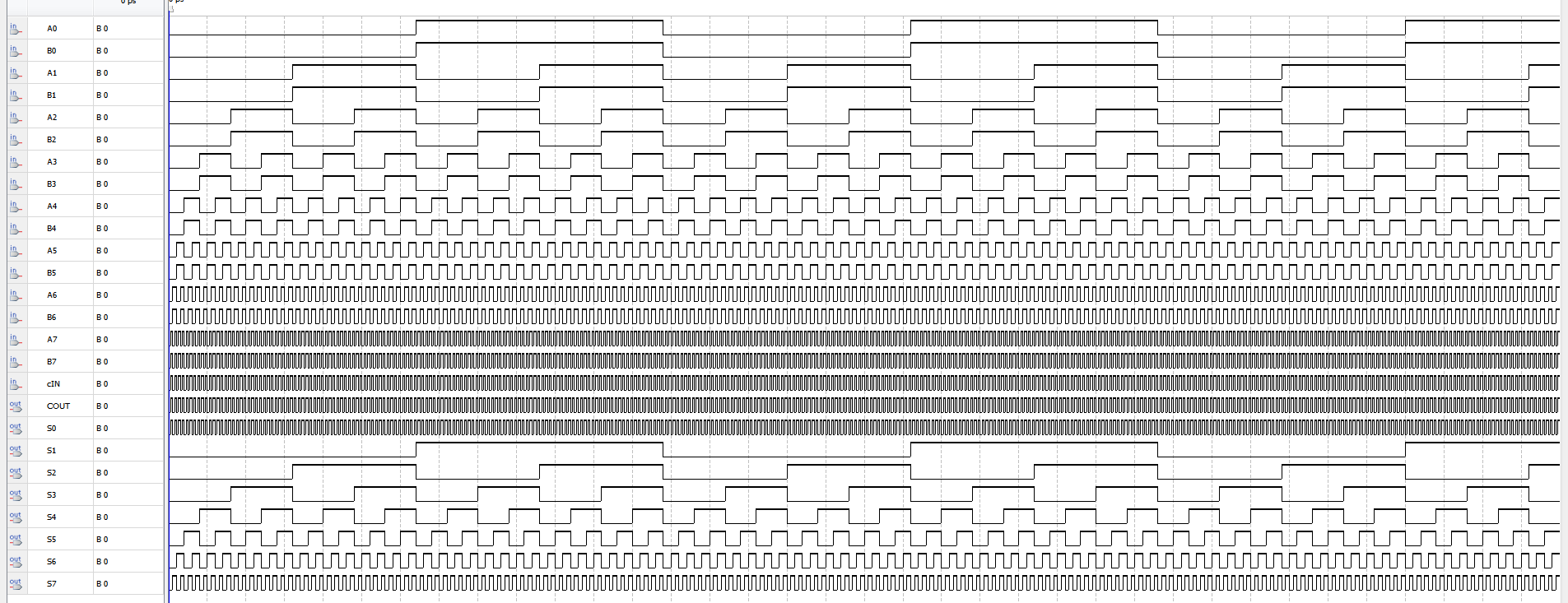
**Discussion and Conclusions**

The objective of this experiment was to create, simulate and program a full adder circuit, and a parallel adder. We first predict the outcome theoretically by determining the output for every possible input combination including a carry input. Then experimentally determine if our theoretical predictions are correct. Circuits for performing binary arithmetic are based on half adders, which add 2 bits, produce a sum and carry. A full adder is like a half adder, however it accounts for a carry input. A parallel binary adder is a group of full adders. With n full adders allowing two n-bit numbers to be added, generating an n-bit sum and a carry output. Our experiment confirmed our predictions from the pre-lab. We did not have any deviations from the expected results, however due to time constraints we were unable to run the experiment for Part III.

**Appendix (Pre-Lab)**

See the following pages for the pre-lab predictions written for this lab.

**Part II – Parallel Adder**

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**Figure 2.2:** Screen-shot of the simulation output of the parallel adder circuit.